A Method for Overlay Metrology of Low Contrast Features

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication and, more particularly to a method for measuring alignment marks in semiconductor fabrication.

BACKGROUND OF THE INVENTION

The use of alignment marks to measure and control the overlay accuracy of various layers in semiconductor processing is well known. Traditionally, optical detection and measurement of the alignment marks has been employed. A top layer is aligned to underlying layers by detecting the overlay variation between an alignment feature that has previously been formed on the underlying layer(s) and an alignment feature that is formed in a photoresist layer on the top layer. Oftentimes a box in a box pattern is employed, such as illustrated in Figure 1a, with one box having been formed in the underlying layer and the other box having been formed in the resist layer.

As device geometries and features sizes decrease, alignment of the layers becomes increasingly critical and tolerances become increasingly tighter. Unfortunately, as device geometries and feature sizes decrease, detection and measurement of the alignment marks becomes more difficult. One reason for this difficulty is that resist lines are transparent and have very small vertical

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